REMARKS

Claims 1-6 and 8-37 are pending in this application. Claims 4, 6, 9-29, 31 and 32 are withdrawn from consideration. Claims 1, 5, 8, 33, 36 and 37 have been amended in order to more particularly point out, and distinctly claim the subject matter to which the applicants regard as their invention.

The support for the claim amendments is as follows: Claims 1, 8, 33, 36, 37 (p.32, lines 20-30) and claim 5 (formal correction). The applicants respectfully submit that no new matter has been added.

The specification has been objected to due to certain informalities, which the Examiner deemed needed correction, as set forth in item 5, page 3 of the outstanding Action. The objections have been addressed by amending the specification in accordance with the Examiner's helpful suggestions.

Claims 36 and 37 are rejected under 35 U.S.C. §112 as being indefinite because of a missing antecedent basis for several elements in the claim (Office Action p.4). Claims 36 and 37 have been amended to address the rejections.

Claims 1-3, 5, 8 and 33-35 are rejected under 35 U.S.C. §103(a) over Shiraishi '746 in view of Lii '304 (Office Action p.4).

Independent claims 1, 8, 33, 36 and 37 have been amended to overcome the obviousness

rejection, by reciting an integrated circuit chip being covered by a layer 2μm or thinner.

Because the function of the IC chip layer in the claimed invention and that of the prior art is completely different, the thicknesses of the IC chip layer are different by design and not different by mere optimization. As will be shown below the IC chip layers of the prior art are not exchangeable with the claimed layer.

Lii'304 is the only reference of the combination disclosing an IC chip layer. (The Office Action noted at the bottom of p.6, "Shiraishi, however, remains silent as to the integrated circuit chip height further including a "layer" as per claims 1-3, 5, 8, 30 and 33-35...") The IC chip layer of Lii'304 is chosen to create a specific compressive stress C to counter balance the tensile stress T along the backside of the silicon die 44, as shown in FIG. 2C. As further explained in the patent,

> The protective layer 48 is chosen to have a relatively high coefficient of thermal expansion, and typically has coefficient of thermal expansion of above 6 ppm/.degree. C. The material of the protective layer 48 may be an organic material such as a plastics material, or a metal such as gold, aluminum, platinum or silver. (Col.3, lines 27-29)
> ...
>
> However, due to the mismatch in the coefficient of thermal expansion of the die 44 and the protective layer 48, the protective layer 48 tends to reduce in size at a faster rate than the die 44 when cooling down, resulting in a compressive stress C developing on the backside.
>
> The tensile stress T combined with compressive stress C cause a resultant tensile stress R, on the backside, which is less than the tensile stress T. Because the resultant tensile stress R is less than the tensile stress T, the likelihood of any surface defects on the backside of the die 44 propagating through the die is reduced.
>
> The following table is based on a model of R/T for different materials and

thicknesses for the protective layer:

	10 μm.	20 μm.	30 μm.
Au	0.81	0.78	0.76
Al	0.91	0.89	0.87
Pt	0.74	0.73	0.72
Ag	0.80	0.76	0.73

The protective layer also fills the cracks. Filling the cracks reduces stress concentration and therefore also the likelihood that the cracks will propagate through the die 44.
(Col. 3, line 60 to col. 4, line 16)

Lii'304 teaches using a protective layer 48 (FIGS. 2B and 2C) of certain materials (mostly metals) of specific thicknesses to create a compressive stress to balance a tensile stress in the silicon die.

The combination of Shiraishi '746 in view of Lii '304 cannot now logically make the claimed invention obvious because the combination would teach a thick protective layer for the purpose of creating compressive stress and filling in cracks in the silicon die. There is no mention in Lii '304 of a IC chip layer 2μm or thinner, for the reason that such a layer would not be able to create the necessary compressive forces based on the dimensions of the die 44 and other components.

In fact, no where in the combination of the references is there discussed a reason for a thinner protective layer, as discussed in the present specification on p.32, lines 15-27:

> Since the gap g between the peripheral side surface of the head IC chip 80 and the inner walls of the recess 241 is 10 to 50 μm and extremely small, the radical

> monomers 127 shown in FIG. 6A cannot easily enter within the recess 241. For this reason, the poly(p-xylylene) layer 110 is formed to a desired thickness of 2 μm on the exposed top and peripheral side surfaces of the main chip body 81, and a thickness of a poly(p-xylylene) layer 110b which is formed on the surfaces of the bumps 84 located inside the recess 241 is suppressed to 1.4 μm which is approximately 30% thinner than the 2 μm poly(p-xylylene) layer 110.

As shown above, there can be no logical combination of Shiraishi '746 in view of Lii '304 for the purpose of teaching a IC chip layer less than 10 μm.

The Examiner is urged to reconsider the rejection in light of the amended claims.

Claims 36-37 are rejected under 35 U.S.C. 103(a) over Shiraishi '746 in view of Grebe '913 (Office Action p.8).

The reasons provided above also apply here in distinguishing over the combination of Shiraishi '746 in view of Grebe '913.

Shiraishi'764 is discussed above and as Office Action notes at the bottom of p.8, the reference, "remains silent as to the integrated circuit chip being "covered at least on the corner portions and bumps mounting the integrated circuit...by a layer of poly(p-xylylene)." Grebe '913 only concerns IC chips in general and there is no disclosure of head slider IC chips which have different structural dimensions.

Grebe '913 discloses the following about the IC chip layer:

> According to the invention the removable first polymeric film 51 on the substrate 11, that is, the layer directly in contact with the solder bumps 41 and the substrate 11, is poly (para-xylylene). The poly (para-xylylene) first polymeric film 51 is from about 3 to 5 microns thick. (Col.6, lines 30-34)

> Parylene is particularly desirable because it is reworkable, dry processable, uniformly depositable by vapor phase deposition, and capable of forming a substantial pin hole free, conformal coating on facing surfaces separated by the 3-5 micron film thickness corresponding to the C4 lift-off distance. (Col.1, lines 36-41).

Thus, Grebe '913 actually discloses two IC chip layers, as shown in FIG. 1, the first one of which being 3-5 μm which corresponds to the C4 (controlled collapse chip connection) lift-off distance.

As shown above, there can be no logical combination of Shiraishi '746 in view of Grebe '913 for the purpose of teaching a single IC chip layer less than 3-5μm, because 3-5μm corresponds to the required C4 lift-off distance. Furthermore, Grebe'913 teaches not one chip layer, but a minimum of two layers as shown in FIG. 1. The reference is actually not related to the claimed technology. The claims as amended and explained above are now free of the rejection of the combination of Shiraishi '746 in view of Grebe '913.

In view of the aforementioned amendments and accompanying remarks, the claims, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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